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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,266	12/14/2001	Kenneth Yi Yun	applied_112	5531

29397 7590 09/30/2005

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EXAMINER	
ROBERTS, BRIAN S	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,266	YUN ET AL.	
	Examiner	Art Unit	
	Brian Roberts	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-41 have been examined.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because they are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

Claims 40 and 41 are objected to because of the following informalities:

- Claim 40 depends on claim 41. For the purpose of examination, the examiner assumes that claim 40 should depend on claim 39.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al. (US 2003/0165151) in view of Chao et al. (US 2002/0061028)

- In reference to claim 1

In Figure 1, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- A queuing device for accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs inherently containing a control channel to supply status messages
- A switch (130) inherently containing a control input for linking switch inputs to switch outputs
- Locking the links to transfer the packet [0049] where locking the links is transferring the packet segmented into cells within the VOQ in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]

Chao et al. (US 2003/0165151) does not explicitly teach accepting information packets having a variable number of cells.

Chao et al. (US 2002/0061028) teaches accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding and/or segmenting the packets into fixed-sized cells upon arrival. [0008]

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method Chao et al. (US 2003/0165151) to include accepting variable length packets that have a variable number of cells based

upon the segmenting and/or padding of the packets into the fixed-sized cells as taught by Chao et al. (US 2002/0061028) because it allows the system to support variable-length packets.

- In reference to claim 2-4

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 1 and 12-13, Chao et al. (US 2003/0165151) further teaches:

- Segmenting variable length packets into fixed-sized cells [0008]
- An arbiter (125) for arbitrating between available switch inputs for the switch output [0050] via a round robin selection method to select the highest priority/least recently used available switch input.
- Locking the links in response to the arbitration process where locking the links is transferring the packet segmented into cells within the VOQ from the switch input to the switch output one cell at a time in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]
- Inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell.

- In reference to claim 5

In Figures 1-3, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- Accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs
- Segmenting variable length packets into fixed-sized cells [0008]
- Arbitrating between available switch inputs for the switch output [0050]
- Selecting the least recently used available switch input via round-robin [0056]
- Locking the links in response to the arbitration process where locking the links is transferring the packet segmented into cells within the VOQ in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]
- Inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell.

Chao et al. (US 2003/0165151) does not explicitly teach accepting information packets having a variable number of cells.

Chao et al. (US 2002/0061028) teaches accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding and/or segmenting the packets into fixed-sized cells upon arrival. [0008]

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method Chao et al. (US 2003/0165151) to include accepting variable length packets that have a variable number of cells based upon the segmenting and/or padding of the packets into the fixed-sized cells as taught

by Chao et al. (US 2002/0061028) because it allows the system to support variable-length packets.

- In reference to claim 6

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 1-3, Chao et al. (US 2003/0165151) further teaches:

- Queuing the new cells as they arrive at the switch into a appropriate VOQ (115) differentiated by the switch outputs to which the information packets are addressed [0041]
- Arbitrating between a plurality of available switch inputs, each available switch input (110) having a virtual output queue (115a-d) addressed to a switch output [0050]

- In reference to claim 7-9

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 1-3, Chao et al. (US 2003/0165151) further teaches:

- A arbitration process using a pointer which moves through entries from highest to lowest priority for each VOQ in a round-robin order [0056]

- The arbitration process inherently occurs over a plurality of arbitration cycles where each arbitrating switch output simultaneously nominates a switch input [0055-57]

- In reference to claim 10

Figure 1, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- Accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs
- Queuing the new cells as they arrive at the switch into a appropriate VOQ (115) differentiated by the switch outputs to which the information packets are addressed [0041]
- Segmenting variable length packets into fixed-sized cells [0008]
- The arbitration process inherently occurs over a plurality of arbitration cycles where each arbitrating switch output simultaneously nominates a switch input [0055-57] where the switch input (110) has a virtual output queue (115a-d) with a packet addressing a switch output
- Using a round robin scheduling to select the least recently used/highest priority switch input [0056].
- A switch (130) for linking switch inputs to switch outputs
- Locking the links to transfer the packet [0049]

- Inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell.

Chao et al. (US 2003/0165151) does not explicitly teach nominating successively lower priority available switch inputs in subsequent arbitration cycles if the nominated switch input is not selected and accepting information packets having a variable number of cells.

Chao et al. (US 2002/0061028) teaches using a round robin selection method to nominate the highest priority switch input and accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding and/or segmenting the packets into fixed-sized cells upon arrival. [0008]

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method of Chao et al. (US 2003/0165151) to accept variable length packets that have a variable number of cells based upon the segmenting and/or padding of the packets into the fixed-sized cells and successively nominate lower priority available switch inputs in subsequent arbitration cycles using a round robin selection method as taught by Chao et al. (US 2002/0061028) if the nominated switch input is not selected because it allows the system to support variable-length packets and it improves the efficiency of the system and prevents the further wasting of network resources on the highest priority switch input by selecting the next highest priority input switch to utilize the network resources.

- In reference to claim 11-15

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 1-3 and 12-13, Chao et al. (US 2003/0165151) further teaches that a switch input contains a plurality of VOQs. Each VOQ corresponds to an arbiter and a switch output. Each switch input request the arbiter that the VOQ pointer is pointing to for access to the switch output. The arbiter chooses the winner from among the requesting input ports. The method inherently involves arbitration and decision cycles.

Chao et al. (US 2003/0165151) does not explicitly teach that a switch input issues a request command for each occupied VCQ when the switch input is not linked to a switch output and selects the switch output corresponding to the last VOQ that was selected in the case where a switch input receives multiple grant commands from switch outputs.

In Figures 3-5, Chao et al. (US 2002/0061028) teaches that each non-empty VOQ associated with a switch input sends a request, a switch output receives the request from the VOQs (410) and selects one VOQ from those VOQs sending request. If the switch input receives multiple grants from multiple switch outputs, one of the candidate grants is selected (540) and a grant is sent to the link associated with the selected one of the candidate grants. (550) The switch input is then linked to the switch output and the cell is transferred. A round robin selection method is used by the switch output to arbitrate the request and the switch inputs to arbitrate the candidate grants.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the request generation and control device of Chao et al. (US 2003/0165151) to include sending request to each arbiter where the VOQ occupancy flag is set then using the round robin scheduling method and current pointer register to grant the particular VOQ that last was selected where the switch inputs receives grant command from a plurality of switch outputs as taught by Chao et al. (US 2002/0061028) because it improves the efficiency of the system by allowing multiple VOQs of a input switch to contend for service at the same time.

- In reference to claim 16

Figure 1, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- Accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs
- Queuing the new cells as they arrive at the switch into a appropriate VOQ (115) differentiated by the switch outputs to which the information packets are addressed [0041]
- Segmenting variable length packets into fixed-sized cells [0008]
- The arbitration process inherently occurs over a plurality of arbitration cycles where each arbitrating switch output simultaneously nominates a switch input [0055-57] where the switch input (110) has a virtual output queue (115a-d) with a packet addressing a switch output

- Using a round robin scheduling and a pointer list to select the least recently used/highest priority switch input [0056].
- A switch (130) for linking switch inputs to switch outputs
- Locking the links to transfer the packet [0049]
- Inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell.

Chao et al. (US 2003/0165151) does not explicitly teach accepting information packets having a variable number of cells and the input switch arbitrating between multiple received nominations received from the output switch.

In Figures 3-5, Chao et al. (US 2002/0061028) teaches accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding and/or segmenting the packets into fixed-sized cells upon arrival [0008] Chao et al. (US 2002/0061028) further teaches a method where each non-empty VOQ associated with a switch input sends a request, a switch output receives the request from the VOQs (410) and selects one VOQ from those VOQs sending request. If the switch input receives multiple grants from multiple switch outputs, one of the candidate grants is selected (540) and a grant is sent to the link associated with the selected one of the candidate grants. (550) The switch input is then linked to the switch output and the cell is transferred. A round robin selection method is used by the switch output to arbitrate the request and the switch inputs to arbitrate the candidate grants. The process simultaneously occurs for each switch input and output.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the request generation and control device of Chao et al. (US 2003/0165151) to include accepting variable length packets that have a variable number of cells based upon the segmenting and/or padding of the packets into the fixed-sized cells and the switch input and output arbitrating method of Chao et al. (US 2002/0061028) because it allows the system to support variable-length packets and improves the efficiency of the system by allowing multiple VOQs of a input switch to contend for service at the same time and for arbitration when multiple request or candidate grants are received by a switch output or input to ensure the highest priority request or candidate grant is selected.

- In reference to claim 17

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 1-3, Chao et al. (US 2003/0165151) further teaches:

- A decision cycle inherently includes a plurality of arbitration cycles
- Locking the links to transfer the packet [0049] and inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell

- In reference to claim 18

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 12-13, Chao et al. (US 2003/0165151) further teaches:

- Using a pointer and a round robin scheduling method to select the highest priority switch input/output during each decision cycle

- In reference to claim 19

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figure 1-3, Chao et al. (US 2003/0165151) further teaches:

- In Figure 2, inherently setting a maximum number of arbitration cycles in each decision cycle and continuing the arbitration cycle until the switch output selects a switch input or a timeout occurs [0053]

- In reference to claim 20, 21

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figure 1-3, Chao et al. (US 2003/0165151) further teaches:

- A winning VOQ has the opportunity to exhaust all of its cells [0056] thus inherently bypassing the arbitration process
- If the winning VOQ only had one cell, it will not submit a request and the outputs pointer will advance thus starting the arbitration process [0056]

- In reference to claim 22

In Figure 1-3, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- Accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs
- Selecting a switch input for each switch output [0050]
- A switch (130) for linking switch inputs to switch outputs
- Locking the links to transfer the packet [0049] where locking the links is transferring the packet segmented into cells within the VOQ in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]
- Repeating the process following transfer reselecting a switch input [0057]

Chao et al. (US 2003/0165151) does not explicitly teach accepting information packets having a variable number of cells or communicating the lengths of the cell.

Chao et al. (US 2002/0061028) teaches accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding and/or segmenting the packets into fixed-sized cells upon arrival. [0008]

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method Chao et al. (US 2003/0165151) to include accepting variable length packets and communicating the length of the packets over a control channel that have a variable number of cells based upon the

segmenting and/or padding of the packets into the fixed-sized cells as taught by Chao et al. (US 2002/0061028) because it allows the system to support variable-length packets and segment the packets into cells for processing.

- In reference to claim 23

In Figure 1 and 12-13, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- A queuing device for accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs having a request generation and control device that inherently contains a control output to supply status messages
- A switch (130) for linking switch inputs to switch outputs inherently in response to commands accepted at a control input
- Locking the links to transfer the packet [0049] where locking the links is transferring the packet segmented into cells within the VOQ in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]

Chao et al. (US 2003/0165151) does not explicitly teach accepting information packets having a variable number of cells or communicating the length of the packets.

Chao et al. (US 2002/0061028) teaches accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding

and/or segmenting the packets into fixed-sized cells upon arrival then reassembling the packets before departure. [0008]

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method Chao et al. (US 2003/0165151) to include accepting variable length packets that have a variable number of cells based upon the segmenting and/or padding of the packets into the fixed-sized cells and then communicating the length of the packet via a control channel as taught by Chao et al. (US 2002/0061028) because it allows the system to support variable-length packets and allows all the cells in the packet to be reassembled before the departure.

- In reference to claims 24-27

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figures 1 and 12-13, Chao et al. (US 2003/0165151) further teaches:

- Segmenting variable length packets into fixed-sized cells [0008]
- An arbiter (125) for arbitrating between available switch inputs for the switch output [0050] via a round robin selection method to select the highest priority/least recently used available switch input.
- Locking the links in response to the arbitration process where locking the links is transferring the packet segmented into cells within the VOQ from the switch

input to the switch output one cell at a time in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]

- Inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell.

- In reference to claim 28

In Figure 1 and 12-13, Chao et al. (US 2003/0165151) teaches a switching system and method that includes:

- A queuing device for accepting packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs having virtual output queues and a request generation and control device that inherently contains a control output to supply status messages
- A switch (130) with packets in virtual output queues, for linking switch inputs to switch outputs inherently in response to commands accepted at a control input
- An arbiter (125) for arbitrating between available switch inputs for the switch output [0050] via a round robin selection method to select the highest priority/least recently used available switch input. The arbiter (125) inherently has a input connected to the queuing device and supplies switch commands to the control input of the switch according to the arbitration
- Locking the links in response to the arbitration process where locking the links is transferring the packet segmented into cells within the VOQ from the switch

input to the switch output one cell at a time in consecutive time slots before any other VOQ of the same input can be served [0049-0050]]

Chao et al. (US 2003/0165151) does not explicitly teach accepting information packets having a variable number of cells.

Chao et al. (US 2002/0061028) teaches accepting variable length packets at a plurality of switch inputs (110) addressed to a plurality of switch outputs and padding and/or segmenting the packets into fixed-sized cells upon arrival. [0008]

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the system and method Chao et al. (US 2003/0165151) to include accepting variable length packets that have a variable number of cells based upon the segmenting and/or padding of the packets into the fixed-sized cells as taught by Chao et al. (US 2002/0061028) because it allows the system to support variable-length packets.

- In reference to claims 29-38

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that inherently includes a timer and covers substantially all limitations of the parent claims.

Chao et al. (US 2003/0165151) does not explicitly teach the arbiter system and arbitration method of claims 29-38.

Chao et al. (US 2002/0061028) further teaches a system with a plurality of arbiters that arbitrate between a plurality of switch inputs and outputs in a plurality of

arbitration cycles where the arbiter contains a priority list for each switch output and utilizes a method of round robin scheduling to issue a candidate grant to the highest priority input switch that the pointer points too. If an input switch receives multiple grant candidates, the arbiter utilizes a round robin method and a pointer to arbitrate between the candidates and accepts the highest priority candidate grant from the switch outputs.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the request generation and control device of Chao et al. (US 2003/0165151) to include the switch input and output arbitrating method and arbiter system of Chao et al. (US 2002/0061028) because it improves the efficiency of the system by allowing multiple VOQs of a input switch to contend for service at the same time and for arbitration when multiple request or candidate grants are received by a switch output or input.

- In reference to claim 39

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that inherently includes a timer and covers substantially all limitations of the parent claims. In Figures 1-3, Chao et al. (US 2003/0165151) further teaches a system that includes:

- A decision cycle inherently includes a plurality of arbitration cycles
- Locking the links to transfer the packet [0049] and inherently transferring the cells in the units of a cell per decision cycle where a decision cycle is defined by the length of time it takes to send a cell

- In reference to 40

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that inherently includes a timer and covers substantially all limitations of the parent claims. In Figure 1-3, Chao et al. (US 2003/0165151) further teaches:

- In Figure 2, inherently setting a maximum number of arbitration cycles in each decision cycle and continuing the arbitration cycle until the switch output selects a switch input or a timeout occurs [0053]

- In reference to claim 41

The combination of Chao (US 2003/0165151) and Chao et al. (US 2002/0061028) teach a system and method that covers substantially all limitations of the parent claims. In Figure 1-3, Chao et al. (US 2003/0165151) further teaches:

- The arbiter that arbitrates between a plurality of switch inputs for a switch output sends commands to lock the switch links so that a winning VOQ has the opportunity to exhaust all of its cells [0056] thus inherently bypassing the arbitration process
- If the winning VOQ only had one cell, it will not submit a request and the outputs pointer will advance thus starting the arbitration process and a new decision cycle [0056]

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Piekarski et al. (US 2002/0141397) teaches a data switch having a virtual queue.
- Sarkinen et al. (US 2003/0058880) teaches a multi-service queuing method and apparatus that provides exhaustive arbitration.
- Divivier (US 2003/0053470) teaches a multicast cell buffer for a network switch.
- Isoyama et al. (US 2001/0021191) teaches a packet switch and method of scheduling.
- Johnson et al. (US 2001/0028659) teaches a data witching arbitration arrangement with VOQs.
- Prabhakar et al. (US 6351466) teaches a switching system and method with VOQs.
- Kamiya et al. (US 2002/0039364) teaches a two-dimensional pipelined scheduling technique with VOQs.
- Magill et al. (US 6915372) teaches a method and apparatus for managing traffic through a buffered crossbar switch fabric.
- Oki et al. (US 6940851) teaches a method of scheduling the dispatch cells in non-empty virtual output queues of multistage switches using a pipelined arbitration scheme.

- Dooley et al. (US 2002/0163922) teaches a network switch port traffic manager having configurable packet a cell servicing.
- Golla et al. (US 2002/0176431) teaches a mulitserver scheduling system and method with VOQs.
- Andrews et al. (US 2003/0031193) teaches a scalable weight-based terabit switch scheduling method.
- Alasti et al. (US 2003/0035427) teaches a method and apparatus for arbitration scheduling with a penalty for a switch fabric.
- Krishna et al. (US 6563837) teaches a method and apparatus for providing work-conserving properties in a non-blocking switch.
- Isoyama et al. (US 6570873) teaches a system and method for scheduling reservation of traffic with priority

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Roberts whose telephone number is (571) 272-3095. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BSR
09/21/2005

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600